

**Course Name**: DIGITL LOGIC DES LAB

**Course Number and Section**: **14:332:233:01**

**Experiment**: prelab 5

**Lab Instructor**: ZAHRA AREF

**Date Performed**:

**Date Submitted**:

**Submitted by**: Chance Reyes 225006531

**Course Name**: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Course Number and Section**: **14:332:xxx:xx**

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--------------------------For Lab Instructor Use ONLY--------------------------

GRADE: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

COMMENTS:

**2.1 SR Latch:**

always @(s, r)

begin

if (s == 1'b0 && r == 1'b0)

begin

q <= q;

qbar <= qbar;

end

else if (s == 1'b0 && r == 1'b1)

begin

q <= 1'b0;

qbar <= 1'b1;

end

else if (s == 1'b1 && r == 1'b0)

begin

q <= 1'b1;

qbar <= 1'b0;

end

else if (s == 1'b1 && r == 1'b1)

begin

q <= 1'bx;

qbar <= 1'bx;

end

end

**2.1 Testbench:**

module SR\_latch\_tb();

reg s, r;

wire q, qbar;

SR\_latch uut (.s(s), .r(r), .q(q), .qbar(qbar));

initial begin

s = 0; r = 0; #10;

s = 0; r = 1; #10;

s = 1; r = 0; #10;

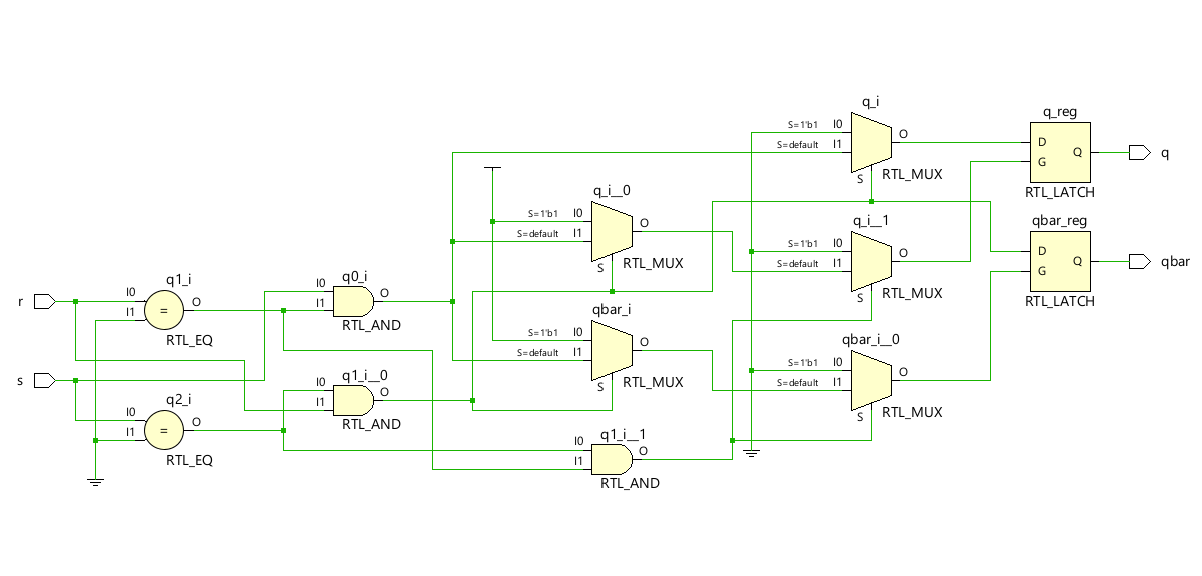
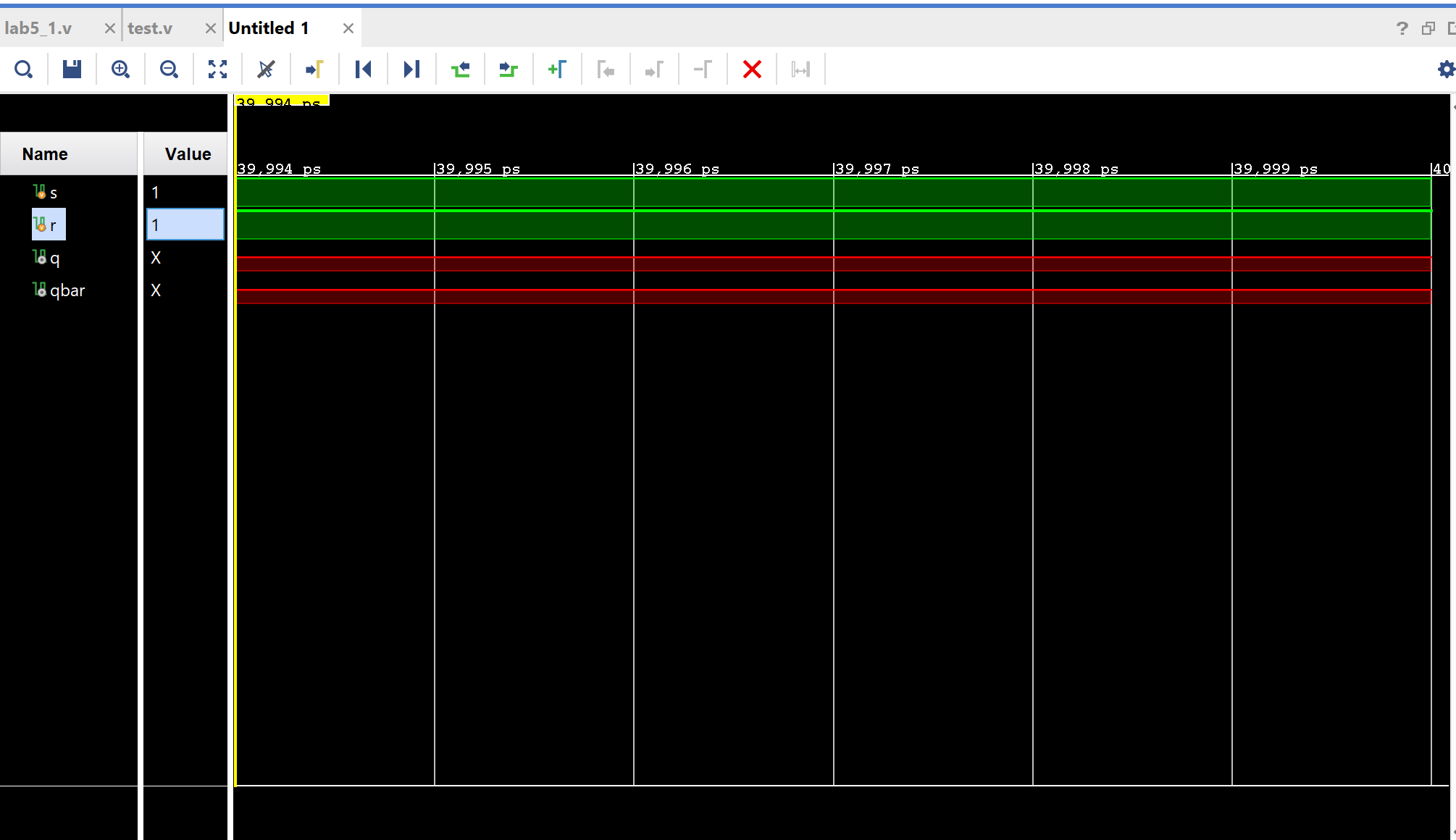
s = 1; r = 1; #10;

$finish;

end

endmodule

**2.1 Schematic & Simulation:**

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**2.2 D Latch:**

module D\_latch(

input d,

input c,

output reg q,

output reg qbar

);

always @(d or c) begin

if (c) begin

q <= d;

qbar <= ~d;

end

end

endmodule

**2.2 Testbench:**

module lab5\_2tb(

);

reg d;

reg c;

wire q;

wire qbar;

D\_latch D\_latch(d,c,q,qbar);

initial begin

c = 0; d = 0; #10;

c = 1; d = 0; #10;

c = 1; d = 1; #10;

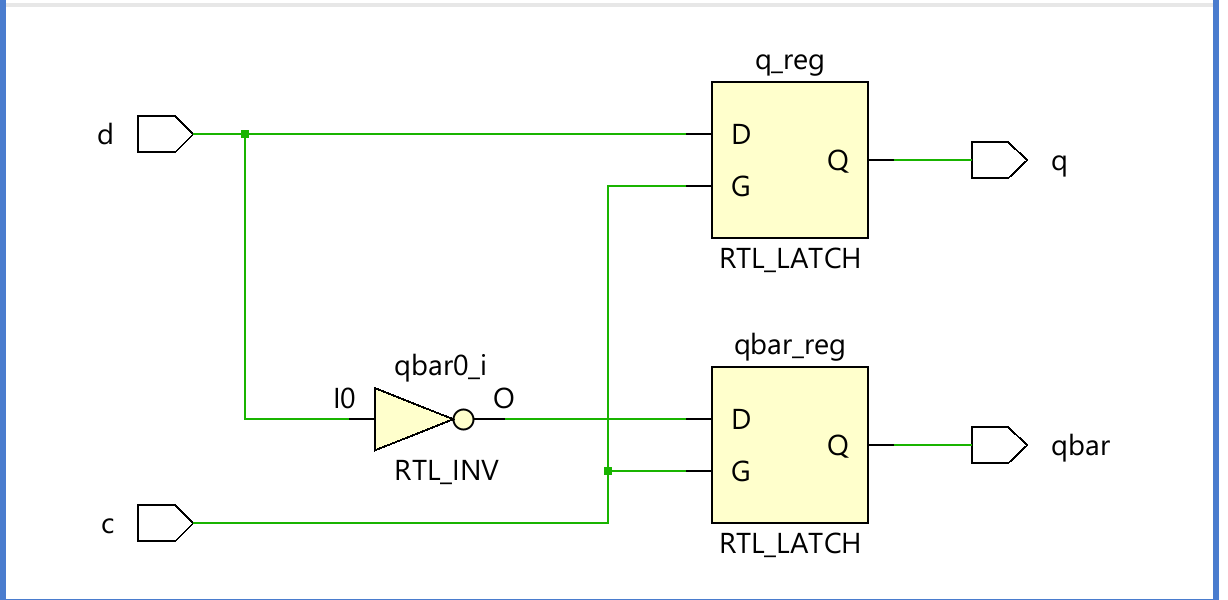
c = 0; d = 1; #10;

$finish;

end

endmodule

**2.2 Schematic & Simulation:**

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